This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2.

Please see the CERN OHL v.1.2 for applicable conditions.
Termination resistors must be placed close to DDR3. A14 is mixed for compatibility with higher memory capacity.

This layout for DDR3 signals was used only to guarantee the PCB design.
You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl).
ALTERNATIVE, NOT MOUNTED BY DEFAULT

Control voltage is +5% VCC. Min. pull range is 10% pm the VCC. Positive slope (Positive voltage for positive frequency shift).

Optional UFL connectors to provide the PCIe mezzanine with a clean clock.

M. Cattin / B. Civel

G.Kasprowicz

Copyright CERN 2014.
OPTIONAL, NOT MOUNTED BY DEFAULT

Stand-alone power port and PCIe interface

Mini DisplayPort connectors for high speed serial links

GTP1

GTP2
Layout Notes:
- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Rf(ESR) connections should be brought from the output to the ground plane.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

DC calculations: Vripple=3xVref
  2.5V: Imax=6A, L=44µH, Rtrip=4.0Ω, R=80Ω, Lloop=3.75A
  1.5V: Imax=6A, L=44µH, Rtrip=4.0Ω, R=80Ω, Lloop=1.5A

Power supplies:
- PUV2
  FPGA 1.3V
  DDR 1.7V
  DDR IO bank 1.2V

- PUV3
  FPGA 1.5V
  DDR 1.7V
  DDR IO bank 1.2V

- TPS53126
  VIN 15V
  PGND 0V
  PGOOD 2.5V

- TPS54110
  VIN 3V3
  PGND 0V
  PGOOD 2.5V

- IRF9910Pbf
  Drain 2A
  Source 2A
  Gate 100nF

- 1% resistors
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.2.
You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (http://ohwr.org/cernohl).