European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland

Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation without any EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY Satisfactory quality and fitness for a particular purpose. Please see the CERN OHL v.1.1 for applicable conditions.

Control voltage is +1.5V ±1V. Min. pull range is ±10 ppm for ±1V. Positive slope (positive voltage for positive frequency shift).

Optional RC filter for 1-bit DAC from FPGA output. Can be used to fine tune Si571, which has a control voltage input.
The skew between the various LA pairs should be kept as low as possible (≈200ps).
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland

Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles

The capacitor bank recommended for decoupling is described in:
Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug36.pdf). Chapter 5 Board Design Guidelines. Check Table 5-2. Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles and Figure 5-1: Stacking for GTP Power and Signal Layers.

Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.

GTP123 can be clocked from VCXO only.
GTP101 used for both FMC and SATA connector can be clocked either from FMC or VCXO.

Simple PCIe FMC Carrier Board

FPGA GTP transceivers
SATA connectors
VCCIO_1=1.8V

VREF_GN4124

Project/Equipment
Simple PCIe Carrier Board

Device
BE-CO FPGA Carrier Board

Description
FPGA bank 1 PCIe bridge connections

EDA-02189-V4-0

European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland

Rev - Sheet A4 - Page 6 of 17

Use of this information is subject to the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING WITHOUT LIMITATION THE IMPLIED WARRANTIES OF MERCHANTABILITY AND SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.
VCCO_2 = 2V5

IC2C

European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
The buses for DDR3 signals were used only to generate PCB classes.

The Termination resistors must be placed close to FPGA.
This document is an Open Hardware and is licensed under the
CERN OHL v.1.1. (http://ohwr.org/CERN-OHL). This license
permits the free redistribution and use of this document.

3) Access SPI Flash from GN4124
This mode is not used to boot the FPGA, but only to
program the SPI Flash memory from the GN4124.

FPGA boot method selection: BOOT_SELx signals are
driven by GPIO of the GN4124. If the GPIO are not
configured (high-Z), the pull-up defines the default mode:

1) Form SPI Flash default mode:
The FPGA is in Master SPI mode and takes its configuration
from the SPI Flash memory.
BOOT_SEL0=high
BOOT_SEL1=high

2) Form GN4124:
The FPGA is in Slave SPI mode and is configured via the
GN4124 by the device at startup
BOOT_SEL0=high
BOOT_SEL1=low

2) Slave serial
M1=low
M0=high
1) Master SPI (default mode)
M1=high
M0=high

FPGA configuration modes:

1) Master SPI (default mode)
M1=high
M0=high

2) Slave serial
M1=low
M0=high

SPIR, JTAG, and configuration signals are not used configuration
signals from the GN4124.
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland

According to PCIe specifications, AC coupling capacitors must be comprised between 75nF and 200nF.

The PCI Express receive inputs on the GN4124 (PERp[3:0]/PERn[3:0]) can be connected using either the advertised polarity, or an inverted polarity. Inverted polarity may be chosen in order to simplify the PCI layout by avoiding signal crossover and additional via.
SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.

configured with the EEPROM content.

*Termination resistors must be placed close to FPGA.

*Termination resistors must be placed close to GN4124.

*Termination resistors must be placed close to FPGA.

*Termination resistors must be placed close to GN4124.
European Organization for Nuclear Research
CH-1211 Geneva 23, Switzerland

Project/Equipment: Simple PCIe Carrier Board

Copyright CERN 2011.
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

DO NOT CONNECT EXTERNAL POWER SUPPLY WHEN THE BOARD IS PLUGGED IN A PCIe SLOT!
DC/DC calculations, Vo=150V:
1.2V, Imax=3A, L=1.54uH, Rtrip=925, C=99.21uF, ILpeak=7.5A
1.8V, Imax=4.5A, L=1.46uH, Rtrip=925, C=99.21uF, ILpeak=7.5A
2.5V, Imax=6A, L=1.41uH, Rtrip=925, C=99.21uF, ILpeak=9A
3.3V, Imax=5A, L=2.59uH, Rtrip=925, C=99.21uF, ILpeak=7.5A

LAYOUT NOTES:
- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions.
- The Kelvin connections should be brought from the output to the feedback pin (FBs) of the device.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
The LVDS receiver can be used to feed a "custom white rabbit copper SFP".

For SFP, Vih = 2.5V so it can be driven from 2.5V supplied FPGA port.