CC-ended lines are named, because Altium Designer treats only P and N ended line names as a differential pair.
For normal use, don't mount C24 and C25.

For testing purposes, remove C24 and C25 and solder C22 and C23. Clock needs to be delivered via the main LA01 pair.

For normal use, don't mount C24 and C25.

Signal frequency from DCO (CLK0_M2C) is given by the following equation:

$$F_{dco} = \frac{F_{sampling} \times \text{bits per sample}}{\text{lines per channel}} / 2$$

F_dco - frequency of DCO signal
F_sampling - ADC sampling frequency
bits_per_sample - 14 (typical) or 16 (compatibility mode)
lines_per_channel - 1 or 2 (typical) pairs per each channel

For example:

$$F_{dco} = \frac{100MSPS \times 14}{2}$$

F_dco = 350MHz

For 16 bit output word length:

$$F_{bit} = \frac{F_{sampling}}{14}$$

For 14 bit output word length:

$$F_{bit} = \frac{F_{sampling}}{12}$$
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

This is necessary to achieve and extend offset correction and then digitally scale it down by factor known after.

DACs and Vref source for offset correction

VREF is 5V.

Resistor R120 added in series with feedback resistors (in the DAC) extends output voltage range of the DAC. This is necessary to achieve and extend offset correction and then digitally scale it down by factor known after.
Warning!
Following the VITA 57.1 standard:
GA0 goes to A1
GA1 goes to A0

Threshold voltage:
- 1V
input voltage range for normal operation:
min. 1.65V (1.3V with 500Ohm termination on both ends of the cable, so divided by 2)
max. 5V with termination on both ends of the cable
Input is +/- 7.5V tolerant for continuous overload and +/-10V tolerant for short term overload.
Si570 is driven by separate I2C interface. It's because there is no possibility of externally setting the last significant bits of the base address (like in case of for example EEPROM memory). So, if two mezzanine cards are plugged to the carrier, conflict on I2C bus appears.

Base address: 0x55 - 1 0 1 0 1 0 1
Maximum voltage:

** ** 600Ohm termination not active **

Normal use: Input voltage must be kept in the range of +/-10V, where the maximum AC value is +/-5V.

Overload: +/-25V. This is the maximum MOSFET switches voltage

** ** 500Ohm termination switched on **

Normal use: Maximum input voltage is +/-7.5V, where the maximum AC value is +/-5V.

Overload: +/-7.5V. This restriction is caused by MOSFET which is series with 470ohm terminating resistor.

Overload may take only short time. Otherwise it may cause input resistors overheat even if input voltage or current is in the MOSFET switch box tolerance.
L7 & L10 are replaced by 390 nH in 603 package.

Components creating is in progress.
Components creating is in progress.

L12 & L13 are replaced by 390 nH in 603 package.
Components creating is in progress.

L15 & L16 are replaced by 390 nH in 603 package.

Project/Equipment: FmADC100M14b4ch

Input stage 4

Amplifier and trigger receiver

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-02063-V2-0
VADJ is set to 2.5V because:
- there is no need of level matching for DAC
- FMC board could be tested with Xilinx kit, where VADJ is fixed to 2.5V

+5.5V is used as a power supply for offset creating DACs. The real value is 6V - 0.6...0.7V which gives 5.3...5.4V. It is lower than 5.5V - max. voltage for normal operation.
Switches configuration:

<table>
<thead>
<tr>
<th>Switch 1</th>
<th>Switch 2</th>
<th>Switch 3</th>
<th>Switch 4</th>
<th>Switch 5</th>
<th>Switch 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWW - LA20_P</td>
<td>SW20 - LA09_N</td>
<td>SW17 - LA11_P</td>
<td>SW19 - LA20_N</td>
<td>SW8 - LA20_P</td>
<td>SW18 - LA11_N</td>
</tr>
<tr>
<td>SW22 - LA02_P</td>
<td>SW26 - LA04_P</td>
<td>SW25 - LA06_P</td>
<td>SW26 - LA04_N</td>
<td>SW8 - LA08_P</td>
<td>SW24 - LA04_P</td>
</tr>
</tbody>
</table>

100mV range: on, on, off, -
1V range: on, off, off, -
10V range: on, off, off, -
DC offset error calibration: off, off, off, on
50Ohm termination: - , - , on , - , -

Trigger:

| LA17_CC_P | LA17_CC_N |
| LA00_CC_P | LA00_CC_N |
| LA01_CC_P | LA01_CC_N |
| CLK2_BIDIR_P | CLK2_BIDIR_N |
| ADC clock | ADC output 1 A |
| ADC output 1 B | ADC output 2 A |
| ADC output 2 B | ADC output 3 A |
| ADC output 3 B | ADC output 4 A |
| ADC output 4 B | ADC output 5 A |

SAMTEC connector
pin assignment

EDA-02063-V2-0

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland